

CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters Patent is:

- 1 1. A method of forming an electrical contact to a
2 silicon-containing substrate comprising the steps
3 of:

4 (a) forming an alloy layer having the formula MX
5 over a silicon-containing substrate, wherein M is a
6 metal--selected from the group consisting of Co and
7 Ni and X is an alloying additive;

8 (b) annealing said alloy layer at a temperature
9 sufficient to form a metal alloy silicide, MXSi,
10 layer; and

11 (c) removing any remaining alloy layer.

1 2. The method of Claim 1 further comprising pre-
2 annealing the alloy layer prior to step (b) at a
3 temperature sufficient to form a metal rich alloy
4 silicide, M₂XSi, layer.

1 3. The method of Claim 1 further comprising a second
2 annealing step after step (c) which is conducted at
3 a temperature that converts the MXSi layer into a
4 metal alloy disilicide, MXSi₂, layer.

1 4. The method of Claim 1 further comprising forming an
2 optional barrier layer over said alloy layer prior

- 3 to step (b), wherein said optional barrier layer is
4 removed by step (c).
- 1 5. The method of Claim 1 wherein said alloying additive
2 is selected from the group consisting of C, Al, Si,
3 Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Ge, Y, Zr, Nb,
4 Mo, Ru, Rh, Pd, In, Sn, La, Hf, Ta, W, Re, Ir, Pt,
5 Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu
6 and mixtures thereof.
- 1 6. The method of Claim 5 wherein said alloying additive
2 is C, Al, Si, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Ge,
3 Y, Zr, Nb, Mo, Ru, Rh, Pd, In, Sn, La, Hf, Ta, W,
4 Re, Ir or Pt.
- 1 7. The method of Claim 6 wherein said alloying additive
2 is Si, Ti, V, Cr, Ni, Ge, Nb, Rh, Ta, Re or Ir.
- 1 8. The method of Claim 1 wherein said alloying additive
2 is present in said alloy layer in an amount of from
3 about 0.01 to about 50 atomic %.
- 1 9. The method of Claim 8 wherein said alloying additive
2 is present in said alloy layer in an amount of from
3 about 0.1 to about 20 atomic %.
- 1 10. The method of Claim 1 wherein M is said alloy layer
2 comprises a Co alloy.
- 1 11. The method of Claim 4 wherein said optional oxygen
2 barrier layer is composed of TiN.

- 1 12. The method of Claim 1 wherein said silicon-
2 containing substrate comprises a single crystal Si,
3 polycrystalline Si, SiGe, amorphous Si, or a
4 silicon-on-insulator (SOI).
- 1 13. The method of Claim 1 wherein said alloy layer is
2 comprised of a single phase.
- 1 14. The method of Claim 13 wherein said single phase is
2 a face centered cubic phase.
- 1 15. The method of Claim 2 wherein said pre-annealing
2 step is carried out using rapid thermal annealing
3 (RTA).
- 1 16. The method of Claim 15 wherein said RTA is carried
2 out at a temperature of from about 350° to about
3 450°C for a time period of from about 10 to about
4 300 seconds.
- 1 17. The method of Claim 1 wherein said annealing step
2 (b) is carried out by RTA.
- 1 18. The method of Claim 17 wherein said RTA is carried
2 out at a temperature of from about 400° to about
3 700°C for a time period of from about 10 to about
4 300 seconds.
- 1 19. The method of Claim 1 wherein said remaining alloy
2 layer is removed utilizing a wet etch step that
3 includes the use of an etchant that is selective for
4 removing said layers.

- 1 20. The method of Claim 3 wherein said second annealing
2 step is carried out by RTA.
- 1 21. The method of Claim 20 wherein said RTA is carried
2 out at a temperature of from about 700° to about
3 900°C for a time period of from about 10 to about
4 300 seconds.
- 1 22. An electrical contact to a region of a silicon-
2 containing substrate comprising:
- 3 a substrate having an exposed region of a silicon-
4 containing semiconductor material, said silicon-
5 containing semiconductor material being doped with
6 an impurity to provide carriers of holes, electrons
7 or both holes and electrons; and
- 8 a first layer of CoXSi_2 , wherein X is an alloying
9 additive, said alloying additive being present in
10 said first layer in an amount of from about 0.01 to
11 about 50 atomic %,
- 12 said first layer and said silicon-containing
13 semiconductor material forming an interface having a
14 predetermined roughness and being substantially free
15 of Co silicide spikes descending into said silicon-
16 containing semiconductor material.
- 1 23. The electrical contact of Claim 22 wherein said
2 alloying additive is selected from the group
3 consisting of C, Al, Si, Sc, Ti, V, Cr, Mn, Fe, Co,
4 Ni, Cu, Ge, Y, Zr, Nb, Mo, Ru, Rh, Pd, In, Sn, La,

5 Hf, Ta, W, Re, Ir, Pt, Ce, Pr, Nd, Sm, Eu, Gd, Tb,
6 Dy, Ho, Er, Tm, Yb, Lu and mixtures thereof.

1 24. The electrical contact of Claim 23 wherein said
2 alloying additive is C, Al, Si, Sc, Ti, V, Cr, Mn,
3 Fe, Co, Ni, Cu, Ge, Y, Zr, Nb, Mo, Ru, Rh, Pd, In,
4 Sn, La, Hf, Ta, W, Re, Ir or Pt.

1 25. The electrical contact of Claim 24 wherein said
2 alloying additive is Si, Ti, V, Cl, Ni, Ge, Nb, Rh,
3 Ta, Re or Ir.

1 26. The electrical contact of Claim 22 wherein said
2 alloying additive is present in said first layer in
3 an amount of from about 0.1 to about 20 atomic %.

1 27. An electrical contact to a region of a silicon-
2 containing substrate comprising:

3 a substrate having an exposed region of a silicon-
4 containing semiconductor material, said silicon-
5 containing semiconductor material being doped with
6 an impurity to provide carriers of holes, electrons
7 or both holes and electrons; and

8 a first layer of NiXSi, wherein X is an alloying
9 additive, said alloying additive being present in
10 said first layer in an amount of from about 0.01 to
11 about 50 atomic %,

12 said first layer and said silicon-containing
13 semiconductor material forming an interface having a
14 predetermined roughness and being substantially free

15 of Ni silicide spikes descending into said silicon-
16 containing semiconductor material.

1 28. The electrical contact of Claim 27 wherein said
2 alloy additive is selected from the group consisting
3 of C, Al, Si, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Ge,
4 Y, Zr, Nb, Mo, Ru, Rh, Pd, In, Sn, La, Hf, Ta, W,
5 Re, Ir, Pt, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er,
6 Tm, Yb, Lu and mixtures thereof.

1 29. The electrical contact of Claim 28 wherein said
2 alloying additive is C, Al, Si, Sc, Ti, V, Cr, Mn,
3 Fe, Co, Ni, Cu, Ge, Y, Zr, Nb, Mo, Ru, Rh, Pd, In,
4 Sn, La, Hf, Ta, W, Re, Ir or Pt.

1 30. The electrical contact of Claim 29 wherein said
2 alloying additive is Si, Ti, V, Cr, Ni, Ge, Nb, Rh,
3 Ta, Re or Ir.

1 31. The electrical contact of Claim 27 wherein said
2 alloying additive is present in said first layer in
3 an amount of from about 0.1 to about 20 atomic %.

1 32. A method for the formation of a silicide phase in a
2 silicon-containing substrate said method comprising
3 at least a step of forming an alloy layer having the
4 formula MX over said silicon-containing substrate,
5 wherein M is a metal selected from the group
6 consisting of Co and Ni and X is an alloying
7 additive whereby said alloy layer controls the
8 temperature of formation of various silicide phases.